UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/147,800	11/05/93	SACHS	H 1217250

EXAMINER
DARBE, V

B3M1/0421

ROBERT C. COLWELL
TOWNSEND AND TOWNSEND KHOURIE AND CREW
STEUART STREET TOWER
ONE MARKET PLAZA, 20TH FLOOR
SAN FRANCISCO, CA 94105

ART UNIT	PAPER NUMBER
2302	3

DATE MAILED: 04/21/94

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on 2/7/94 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice re Patent Drawing, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-23 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-23 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

1. The drawings are objected to because they are do not meet required specifications. Correction is required. See Form 948. Applicant is required to submit a proposed drawing correction in response to this Office action. However, correction of the noted defects can be deferred until the application is allowed by the examiner. In addition, applicants should review all drawings for errors, such as typographical errors, inconsistent labels, elements referred to in the specification but not shown in the drawings, elements shown in the drawings but not referred to in the specification, etc.

2. Applicants should ***thoroughly*** review specification for errors, such as typographical and grammatical errors, elements that are discussed but not shown in the drawings, etc. Also, the terminology used in the claims should be consistent with that used in the specification and vice versa.

3. Claims 1-23 rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention as follows:

a. In the expression "in a computing system in which groups of individual instructions are executable in parallel by processing pipelines...", it is unclear if

it is only the individual instructions in a group which are executable in parallel (i.e. only one group at a time is executed) or if more one group is executed in parallel with another group.

b. Claims include elements which have not been positively set forth; e.g. the pipeline of claim 1. *Applicants should review all claims for additional elements or features which have not been positively set forth.*

c. Claims refer to means using a functional recitation that is indefinite because it is not supported by recitation in the claim of sufficient structure to accomplish the function; e.g. the "means responsive to the group identifier for causing all instructions having the same group identifier to be executed at the same time" and the "means responsive to the pipeline identifier of the individual instructions in the group to supply each instruction in the group to be executed in parallel to an appropriate pipeline" of claims 1 and 11, etc. *Applicants should review all claims for additional lack of recitation of sufficient structure to accomplish stated functions.*

d. Applicants are inconsistent or incomplete in their terminology, for example:

i. "storage means" (in claim 1) and "storage" (in claim 11).

ii. Applicants may consider replacing the term "cross-bar" which literally means "horizontal stripe or bar" by the term "crossbar interconnection means" or "crossbar switch" (as in claim 16).

iii. use of the term "pipelines" and "processing pipe-lines" apparently interchangeably, particularly when neither of these elements have been positive-ly set forth (e.g. claim 11).

Applicants should review all claims for additional inconsistencies.

4. Claims 10,11,16, and 23 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. § 112. Claims 12-15,17-19, and 22 would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.
In addition to the rejections above; following are more detailed comments regarding claims 10-23:

a. Regarding claim 10; it is unclear what constitutes a group identifier and pipeline identifier and how they

are associated with a particular instruction. It is unclear how the "group identifier of those instructions to be next executed in parallel" is produced, in order to be compared. Therefore, it is unclear how a comparison of the group identifiers is accomplished. It appears that a single pipeline identifier is used to control an execution unit (pipeline in claim 23). In claim 10, it is unclear whether the execution unit itself contains all the separate pipelines and how the control is accomplished.

b. Regarding claim 11; it is unclear how or what receives instructions in reference to page 24, line 33 since there is not sufficient structure to accomplish this function.

c. Regarding claims 12 and 17; it is stated "the first set of connectors consists of a set of first communication buses, one for each instruction in the storage". The applicants should make sure that their intention is accurately reflected, i.e. a "storage" holding 1000 instructions would therefore have 1000 sets of first communication buses. Also, it is unclear whether or not there is any correlation between a pipeline identifier and a particular decoder in the set. That is, the claim could be interpreted to mean that the decoders

are arranged in a serial manner and that all pipeline identifiers are fed into the first decoder in the set of decoders. It also appears that the set of decoders produce only a single switch signal, effectively activating connection between only one pipeline and the storage.

d. Regarding claim 13; it is unclear to what the detector means is coupled or connected.

e. Regarding claims 14,15,18 and 19; it appears that a multiplexer has been assigned the function of comparing signals. A multiplexer (as understood in this art) is merely a switching apparatus.

f. Regarding claim 16; it is unclear to what the selection means and decoder means are coupled or connected. The term output signal could be interpreted to refer to any signal produced by any of the means given.

g. Regarding claims 20 and 21; it is unclear what constitutes a pipeline identifier and how it is associated with an instruction. It is unclear how a pipeline identifier is used to control the switches, i.e. it appears that all instructions could be switched to a single pipeline. In claim 21, it is unclear to what the number of decoders corresponds.

h. Regarding claim 22; it is unclear how the "group identifier of those instructions to be next executed in parallel" is produced. Therefore, it is unclear how a comparison of the group identifiers is accomplished and of what the output comparison signals consist.

Applicants are advised that they should consider the reasoning behind the rejections of claims under 35 U.S.C. § 102 below when rewriting or amending the claims listed above because of similarities between the claims.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by Iizuka, U.S. Patent No. 5,299,321. Iizuka discloses a computing system which is "a parallel processing device consists of plural processing pipelines arranged in parallel, decoders which decode processing instructions and outputs them to

respective processing pipelines and a general register in which the processing instruction to be outputted to each of decoders is written in one of its registering sections, or a multiple port register". Iizuka shows three embodiments of his invention.

7. Regarding claims 1,2,3,4 and 5; the storage means correlates (in Iizuka's third embodiment) to the two-dimensional expanded instruction register (element 148, figure 3). In this embodiment, the group identifier is disclosed as the "line" address and the pipeline identifier is disclosed as the "column" (Col. 4, line 53 - Col. 5, line 23) which are inherently contained in the two-dimensional expanded instruction register. The group of instructions to be executed in parallel is identified by a field in the parallel execute instruction (element 131, figure 9).

8. Referring to claims 6,7,8 and 9; determining the group identifier and pipeline (and pipeline identifier) is disclosed in Iizuka (Col. 7, line 37 et seq.) as determining which "column" and "row" of the two-dimensional instruction register should hold a particular microinstruction and then subsequently storing the microinstruction in that location. The parallel execute instruction causes the microinstructions to be outputted to the processing pipelines as described in Col. 7, line 65 et seq.

9. Claims 20 and 21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kumar et al., U.S. Patent No. 5,197,137. Kumar discloses a computer system that processes instructions in parallel using a plurality of pipelines. As discussed in Column 6, line 8, et seq., instructions which can be processed in parallel are fed to dispatch units (elements 204..206, figure 1) which expand the instructions into primitive instructions. The instructions in the dispatch units are then routed to the appropriate execution units via a crossbar network. The appropriate execution unit is identified as the execution unit containing the data memory to which a result is to be stored.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure and is as follows:

Emma et al., U.S. Patent No. 5,297,281 shows a digital computer including a main and auxiliary pipeline processor which are configured to concurrently execute contiguous groups of instructions taken from a single instruction sequence.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Valerie Darbe whose telephone number is (703) 305-9839.

12. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

ALYSSA H. BOWLER
SUPERVISORY PATENT EXAMINE
GROUP 2300

VAD
April 14, 1994